

# SLIDES FOR CHAPTER 11

## LATCHES AND FLIP-FLOPS

*This chapter in the book includes:*

Objectives

Study Guide

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11.2 Set-Reset Latch

11.3 Gated D Latch

11.4 Edge-Triggered D Flip-Flop

11.5 S-R Flip-Flop

11.6 J-K Flip-Flop

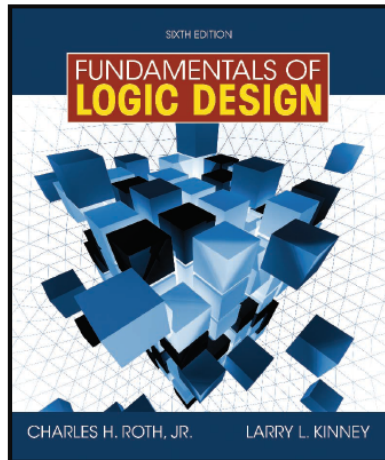
11.7 T Flip-Flop

11.8 Flip-Flops with Additional Inputs

11.9 Summary

Problems

Programmed Exercise



Click the mouse to move to the next page.  
Use the ESC key to exit this chapter.

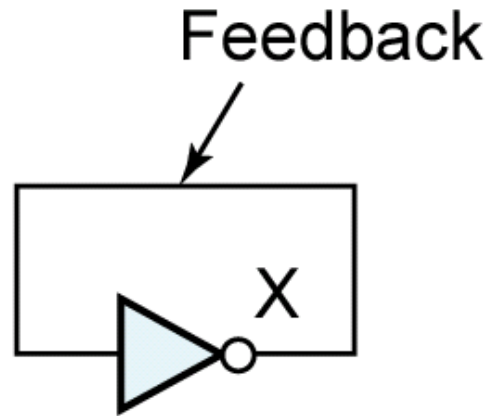
# Sequential Circuits

Sequential switching circuits have the property that the output depends not only on the present input but also on the past sequence of inputs.

In effect, these circuits must be able to “remember” something about the past history of the inputs in order to produce the present output.

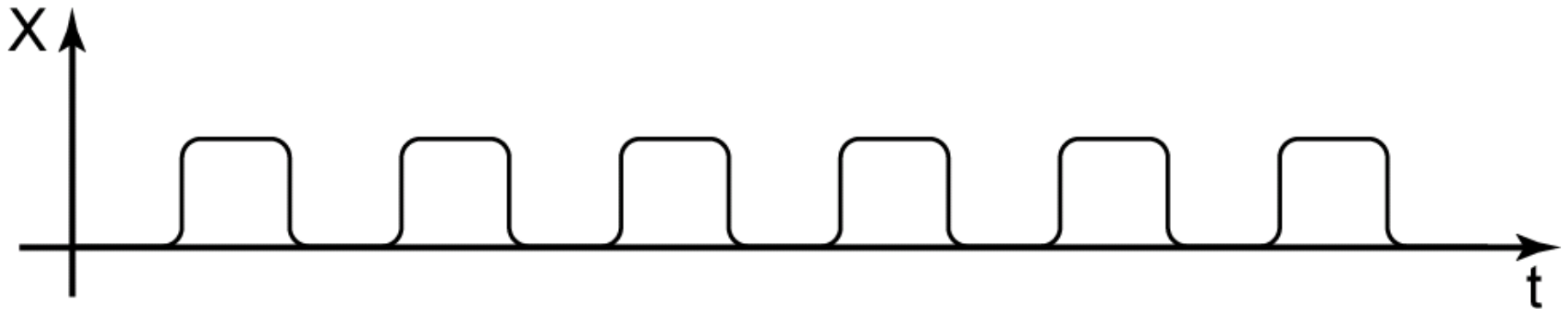
We say a circuit has feedback if the output of one of the gates is connected back into the input of another gate in the circuit so as to form a closed loop.

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Example of a feedback circuit with no stable states.

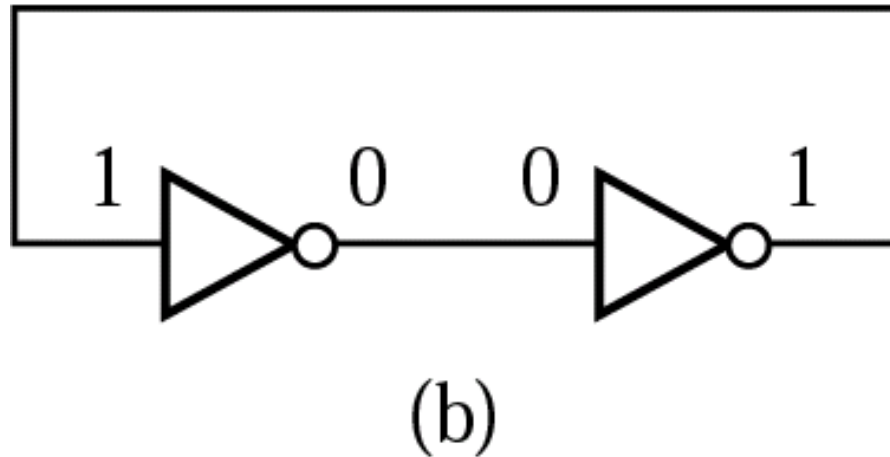
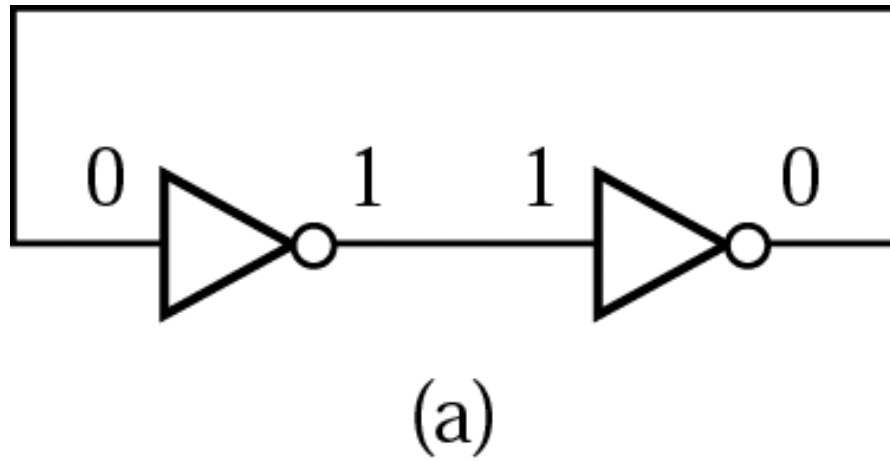
(a) Inverter with feedback



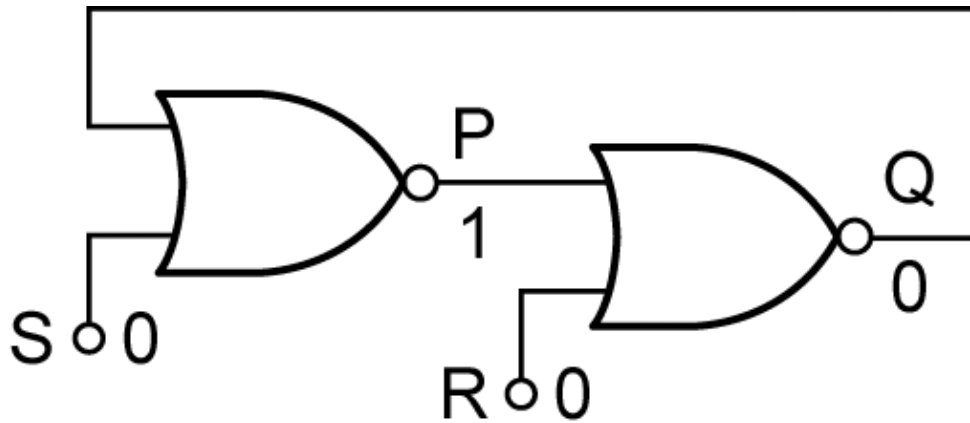
(b) Oscillation at inverter output

**Figure 11-1**

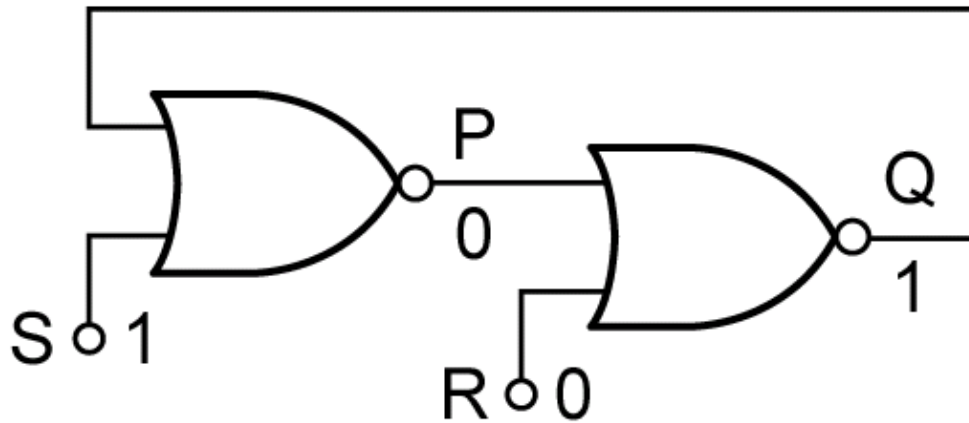
Example of a feedback circuit with 2 stable states.



**Figure 11-2**

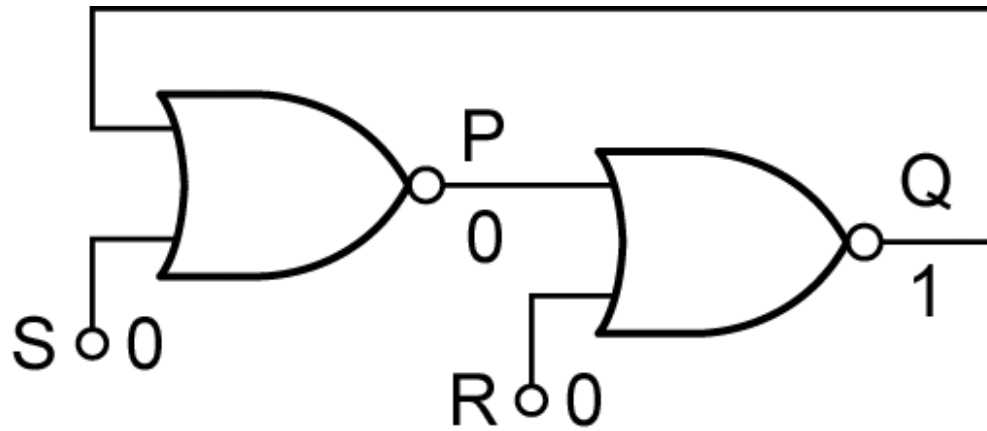


(a)

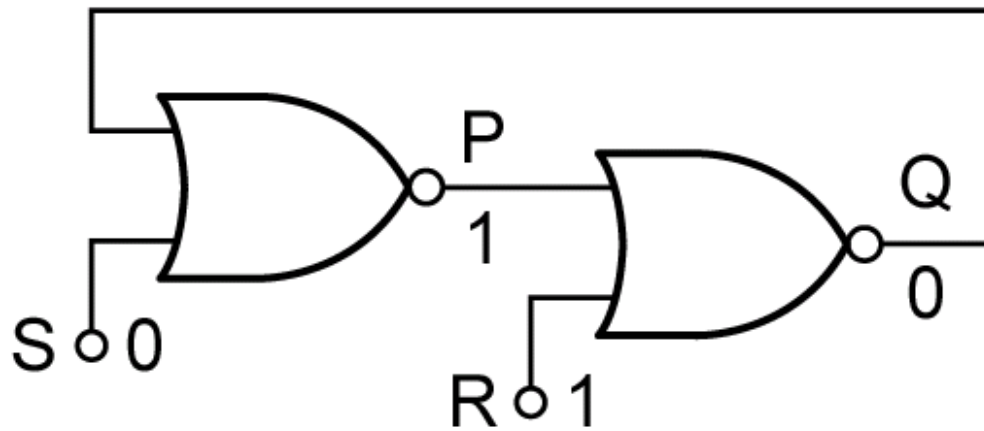


(b)

**Figure 11-3: Set-Reset Latch**

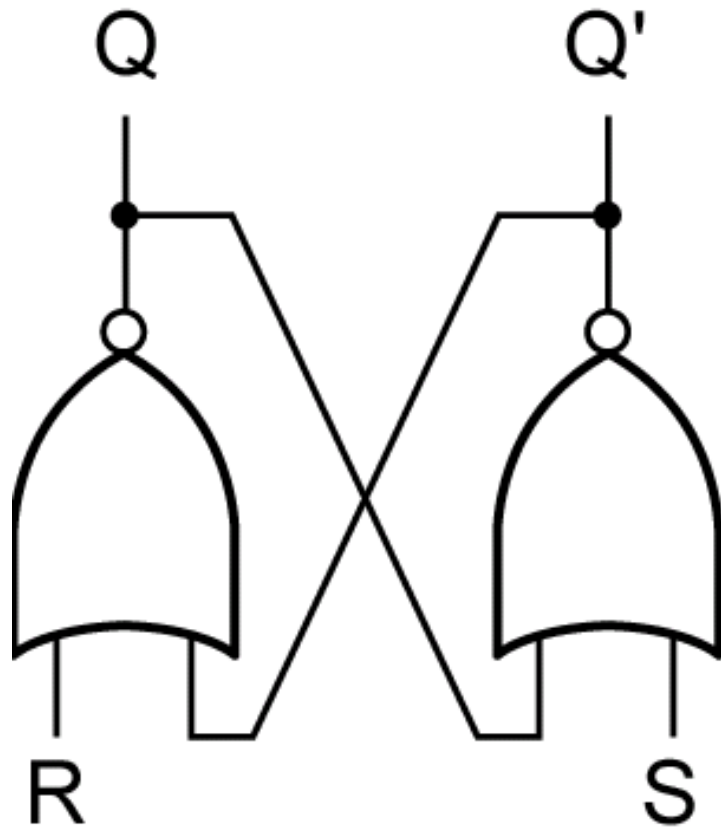


(a)

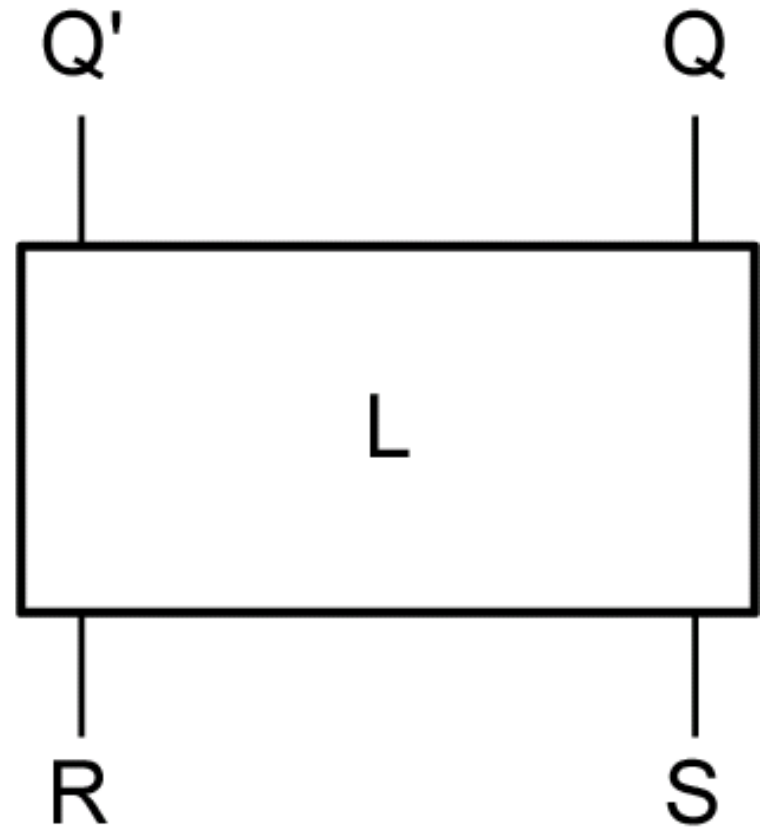


(b)

**Figure 11-4**



(a)



(b)

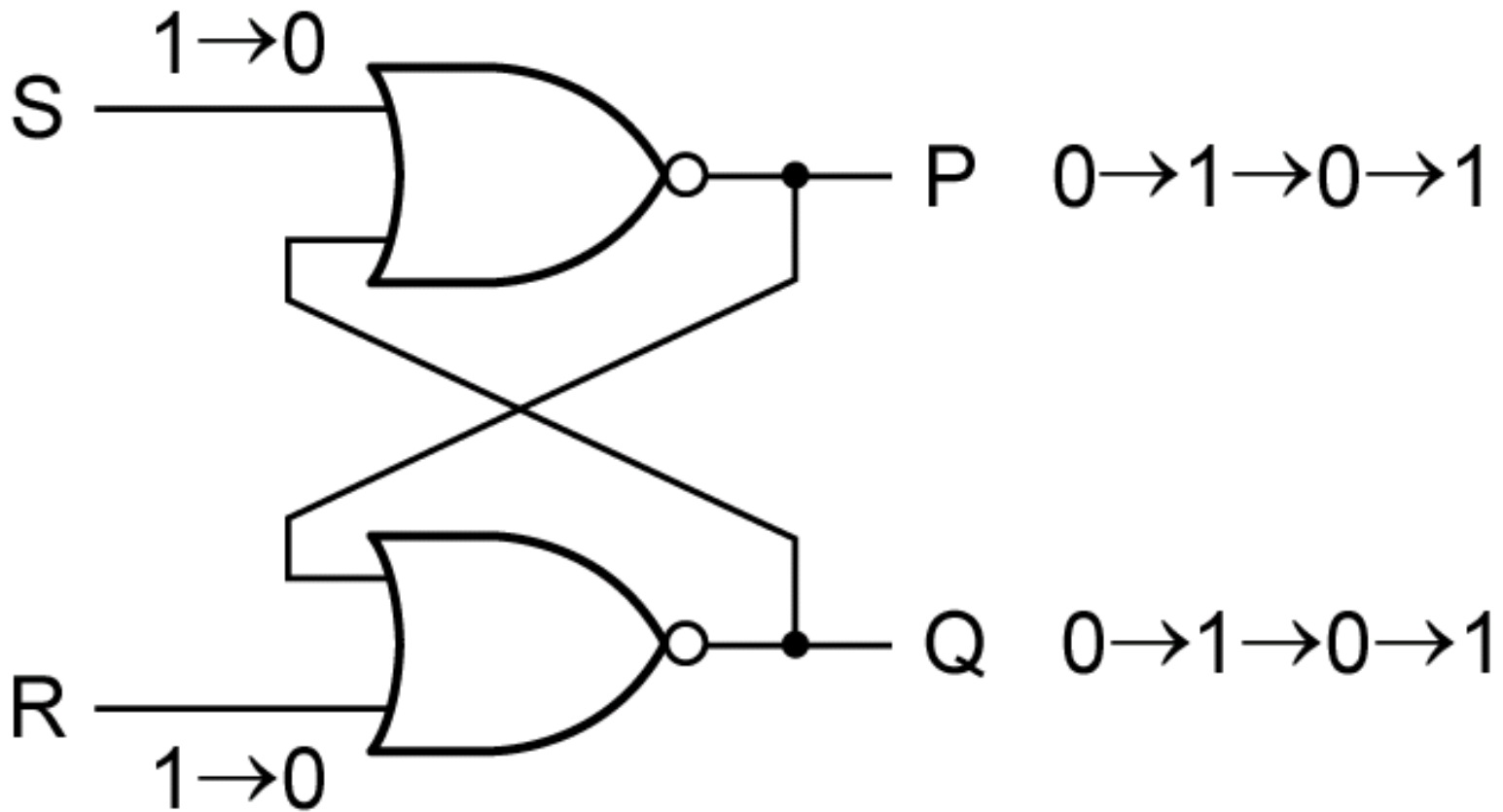
**Figure 11-5: S-R Latch**  
(Set-Reset Latch)

# Set-Reset Latch Behavior

- If  $S = 1$  (Set),  $Q^+ = 1$
- If  $R = 1$  (Reset),  $Q^+ = 0$
- If  $S = R = 0$ ,  $Q^+ = Q$  (no change)
- $S = R = 1$  is not allowed.

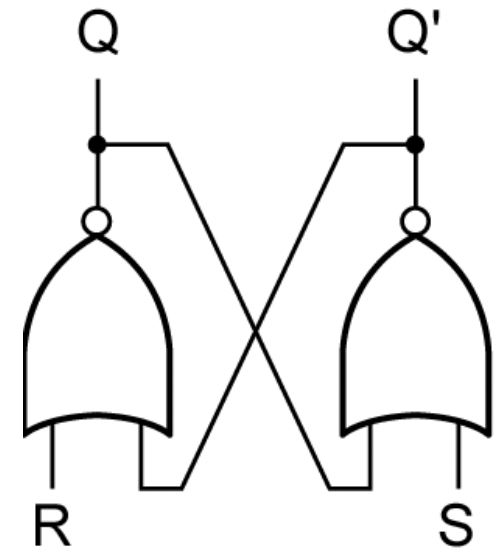
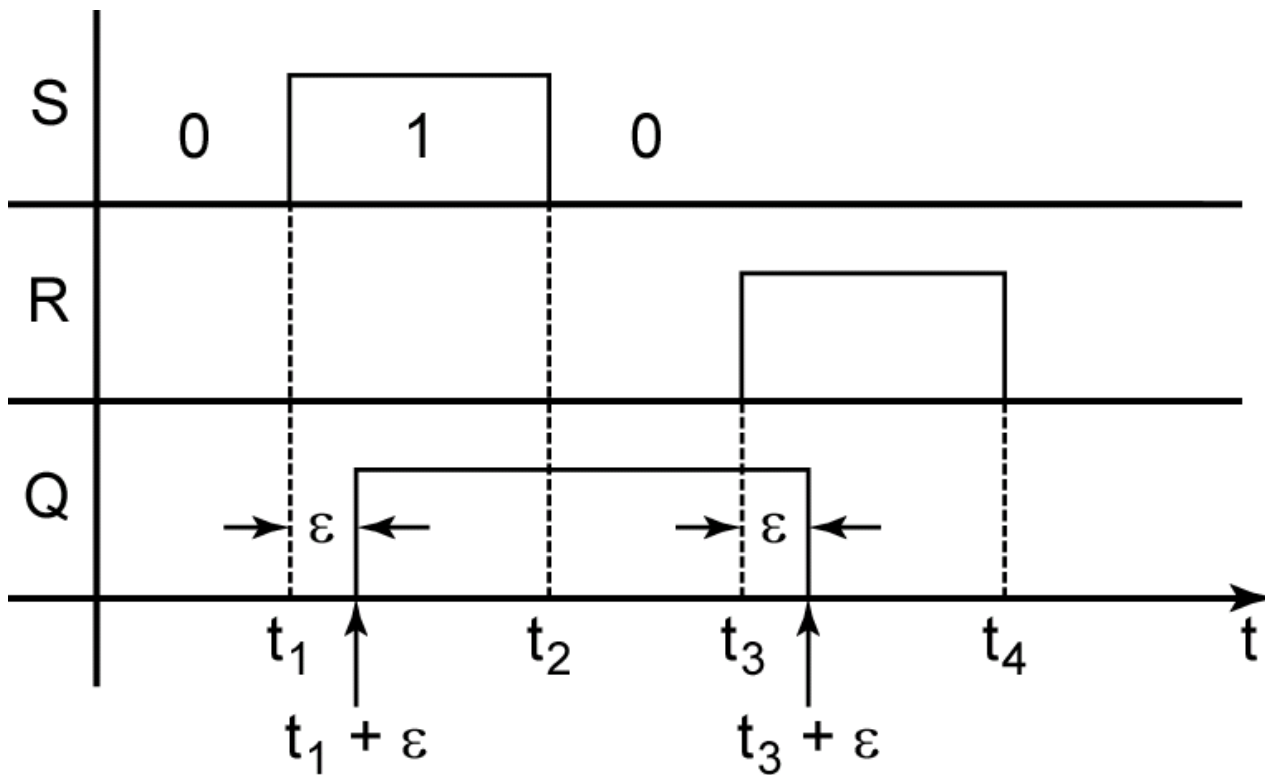
S	R	$Q^+$
0	0	Q
0	1	0
1	0	1
1	1	Not allowed

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**Figure 11-6: Improper S-R Latch Operation**

$$P \neq Q'$$



**S-R Latch**

**Figure 11-7: Timing Diagram for S-R Latch**

## Table 11-1. S-R Latch Next State and Output

Present State Q	Next State $Q^+$				Present Output $P$			
	SR 00	SR 01	SR 11	SR 10	SR 00	SR 01	SR 11	SR 10
0	0	0	0	1	1	1	0	0
1	1	0	0	1	0	0	0	0

Stable states are circled.

Note that for all stable states,  $P = Q'$  except when  $S = R = 1$ . This is one of the reasons  $S = R = 1$  is not allowed.

	$S$	0	1
$RQ$			
00		0	1
01		1	1
11		0	X
10		0	X

$S$	$R$	$Q$	$Q^+$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	—
1	1	1	—

— } Inputs not allowed  
 — }

(a)  $Q^+$  map

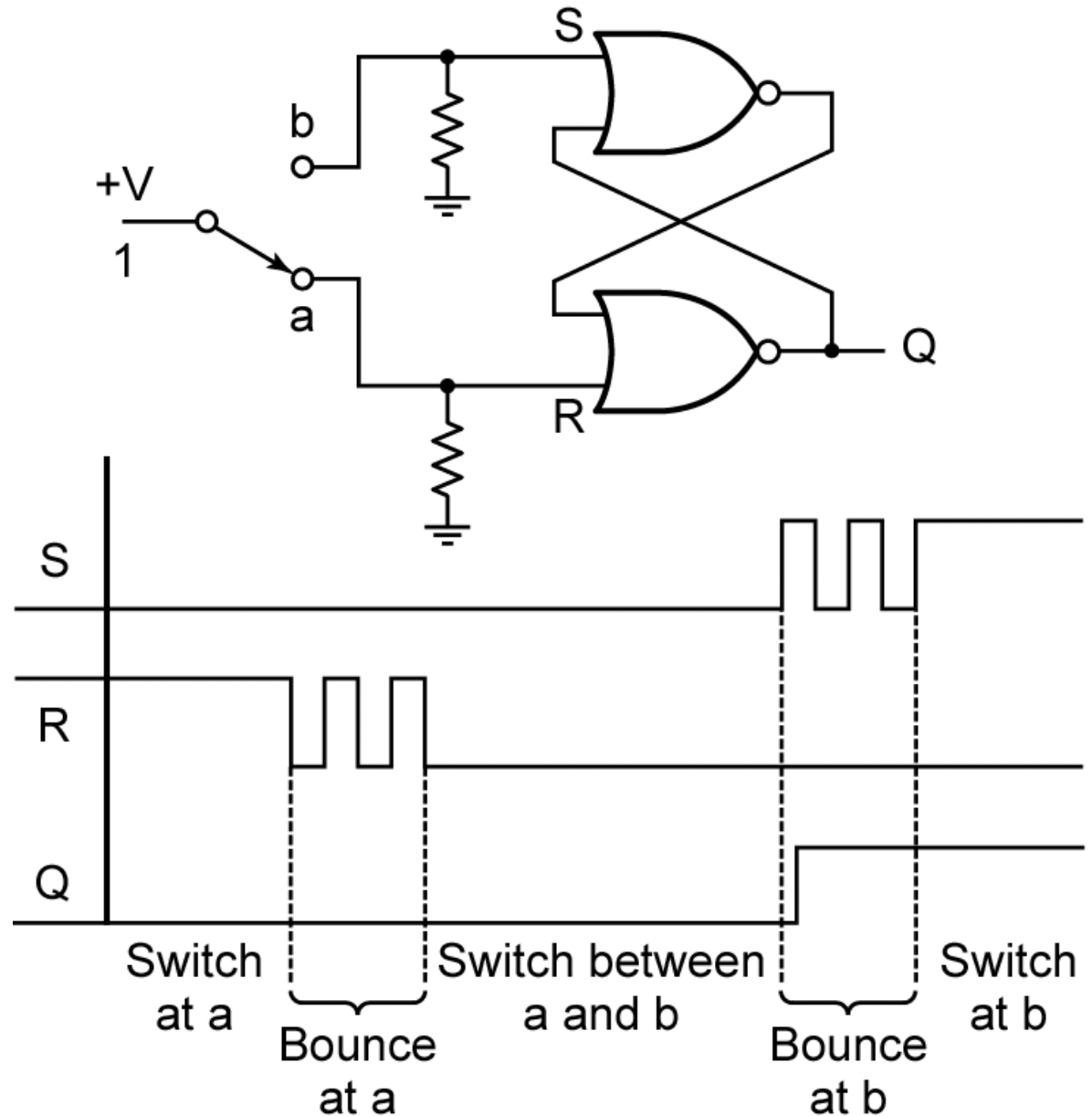
(b) Truth table

$$Q^+ = S + R'Q \quad (SR = 0) \quad (11-5)$$

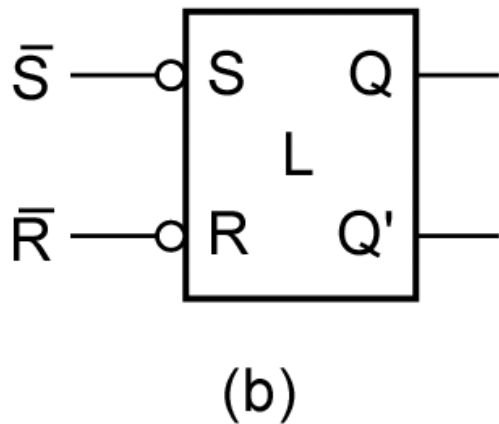
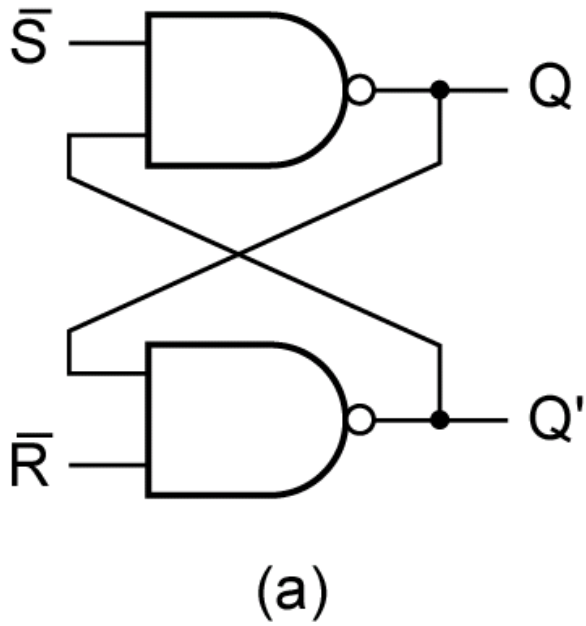
**Figure 11-8: Derivation of  $Q^+$  for an S-R Latch**

Pull-down resistors insure  $S = R = 0$  while switch switches from a to b.

This results in a clean Q signal, even though a and b bounce.



**Figure 11-9: Switch Debouncing with an S-R Latch**



$\bar{S}$	$\bar{R}$	$Q$	$Q^+$
1	1	0	0
1	1	1	1
1	0	0	0
1	0	1	0
0	1	0	1
0	1	1	1
0	0	0	—
0	0	1	—

inputs not allowed

**Figure 11-10:  $\bar{S}$ - $\bar{R}$  Latch**

Alternate form of S-R latch that uses NAND-gates instead of NOR-gates.

# Gated D Latch

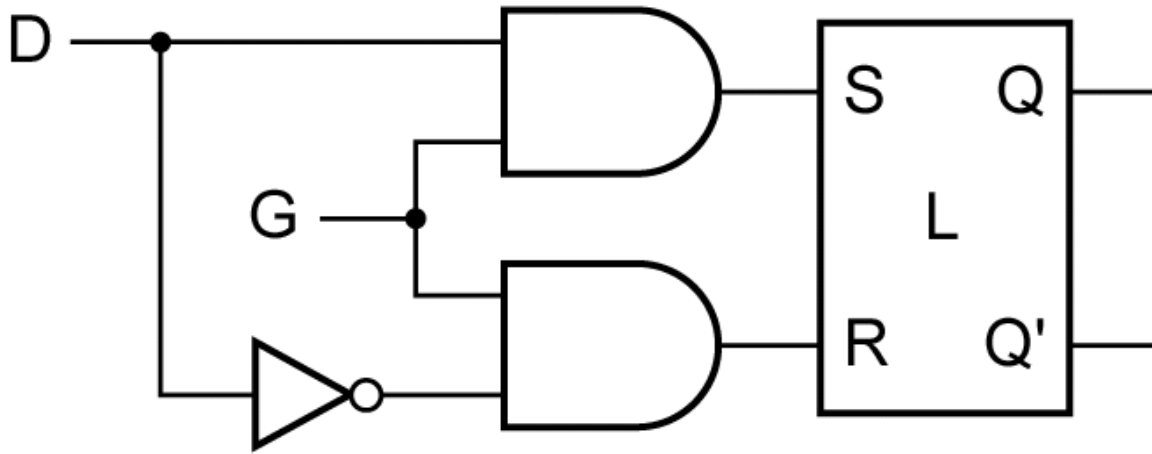
A gated D latch has two inputs – a data input (D) and a gate input (G). The D latch can be constructed from an S-R latch and gates.

When  $G = 1$ , the value of D is passed to Q.

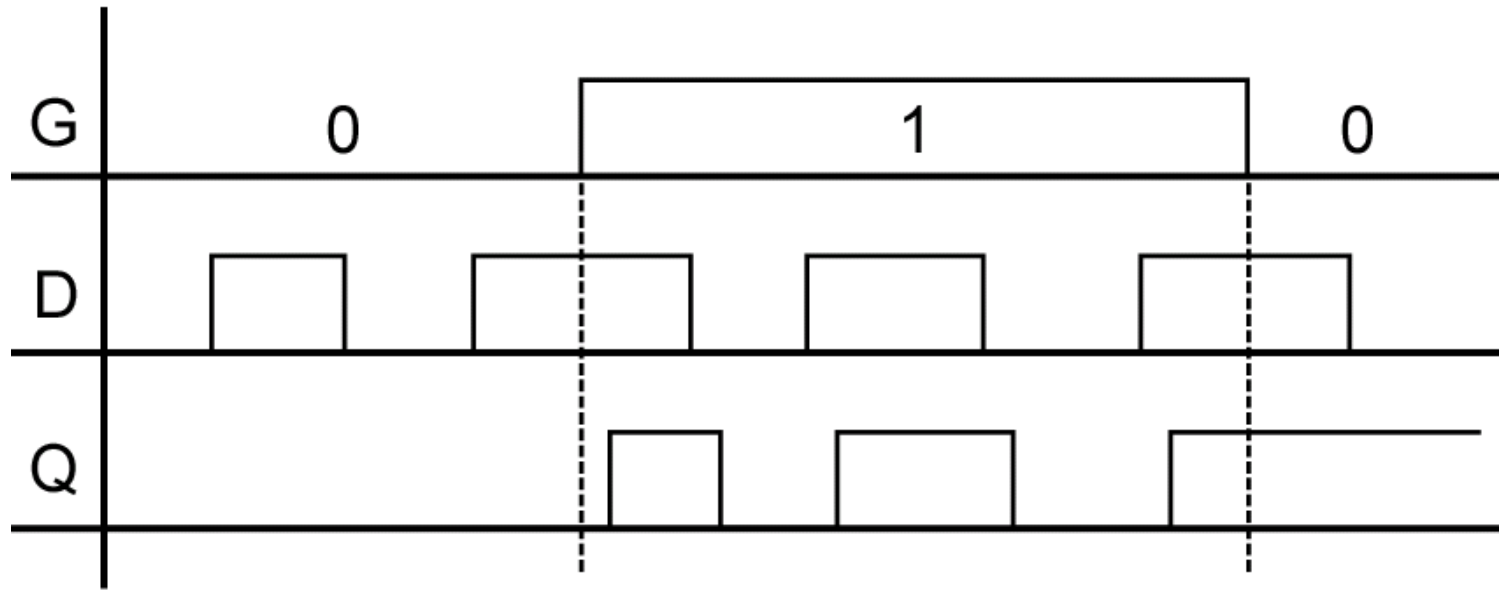
When  $G = 0$ , the Q output holds the last value of D (no state change).

This type of latch is also referred to as a transparent latch.

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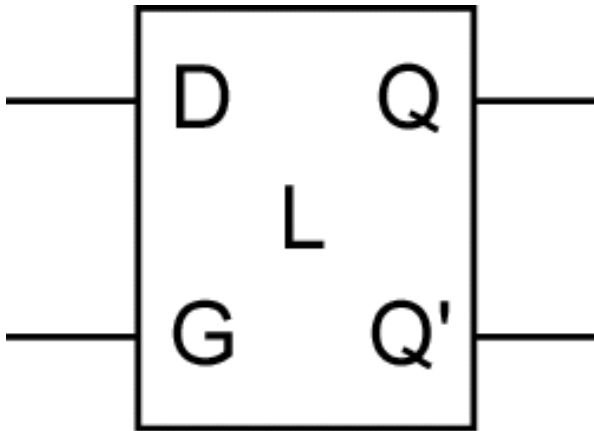


(a)



(b)

**Figure 11-11: Gated D Latch**



$G$	$D$	$Q$	$Q^+$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

**Figure 11-12: Symbol and Truth Table for Gated Latch**

		GD			
		00	01	11	10
Q	0	0	0	1	0
	1	1	1	1	0

$$Q^+ = G'Q + GD$$

**Figure 11-12 (continued)**

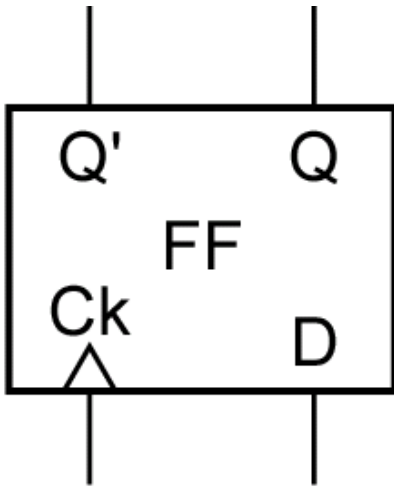
# Edge-Triggered D Flip-Flop

A D flip-flop has two inputs,  $D$  (data) and  $Ck$  (clock). The small arrowhead on the flip-flop symbol identifies the clock input. Unlike the  $D$  latch, the flip-flop output changes only in response to the clock, not to a change in  $D$ .

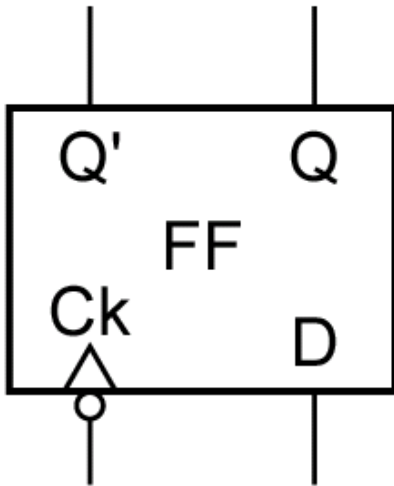
If the output can change in response to a 0 to 1 transition on the clock input, we say that the flip-flop is triggered on the *rising edge* (or positive edge) of the clock.

If the output can change in response to a 1 to 0 transition of the clock input, we say that the flip-flop is triggered on the *falling edge* (or negative edge) of the clock. An inversion bubble on the clock input indicates a *falling-edge trigger*.

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(a) Rising-edge trigger



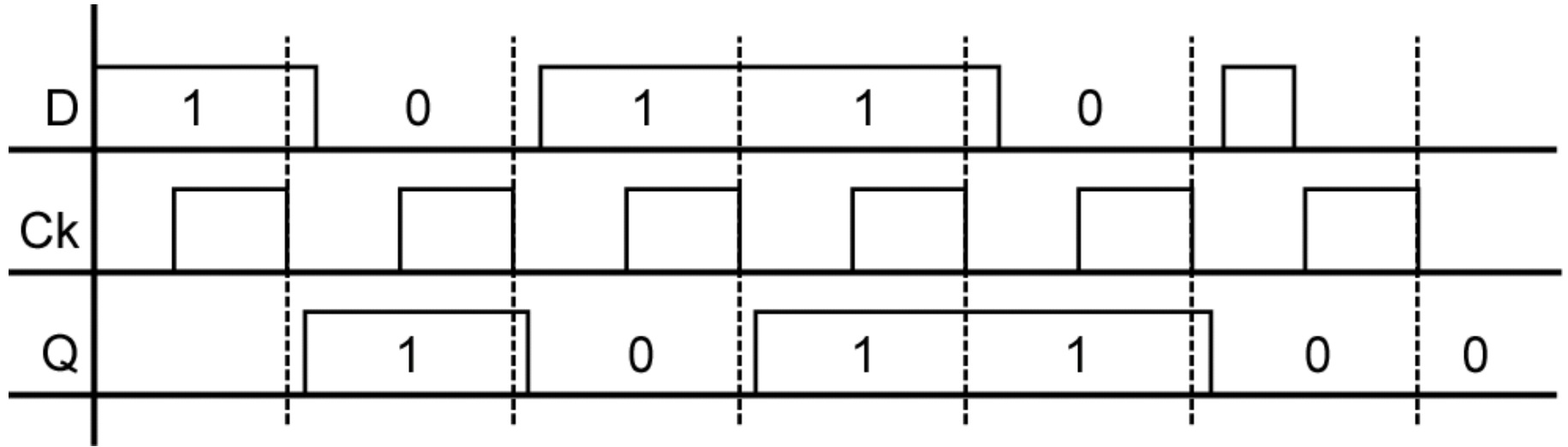
(b) Falling-edge trigger

$D$	$Q$	$Q^+$
0	0	0
0	1	0
1	0	1
1	1	1

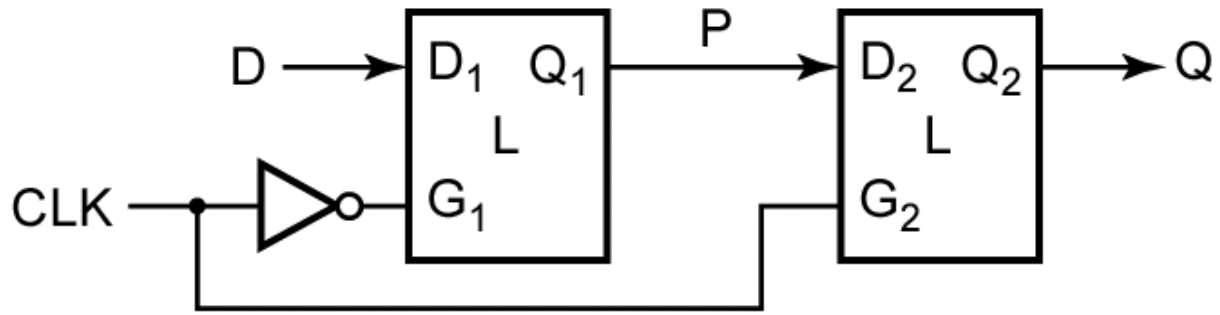
(c) Truth table

$$Q^+ = D$$

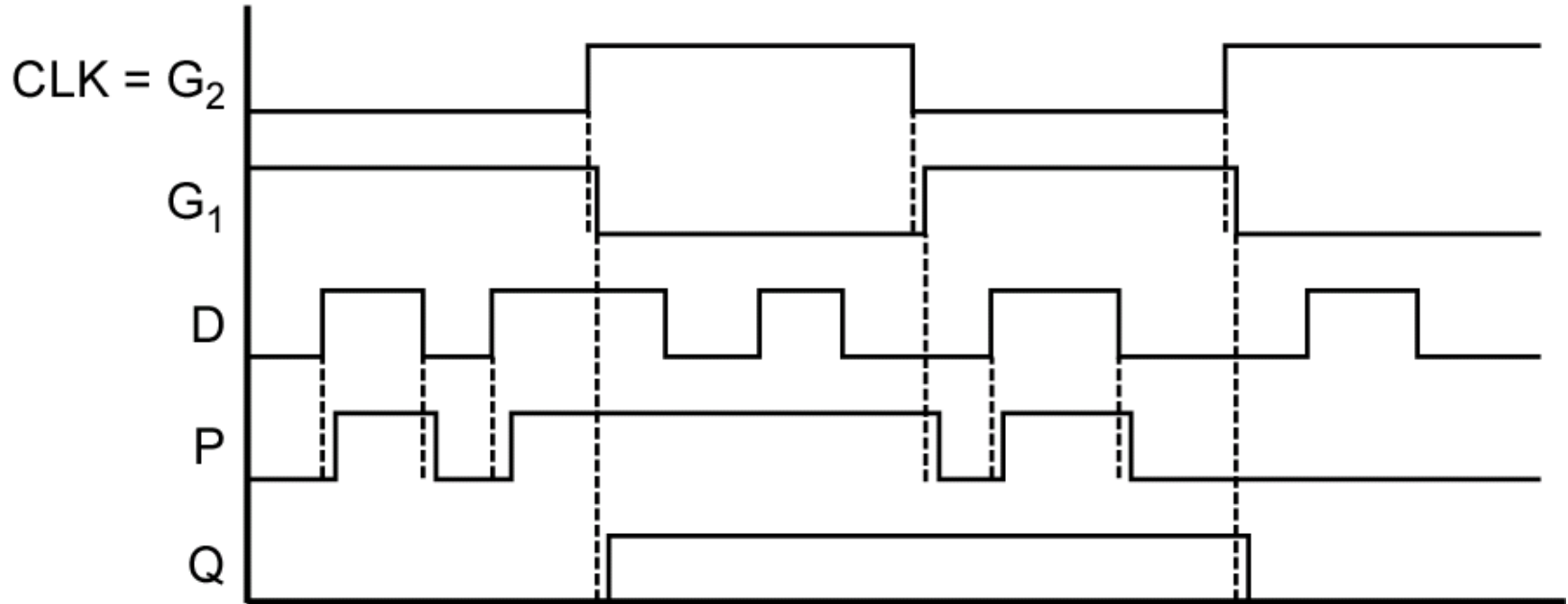
**Figure 11-13: D Flip-Flops**



**Figure 11-14: Timing for D Flip-Flop (Falling-Edge Trigger)**

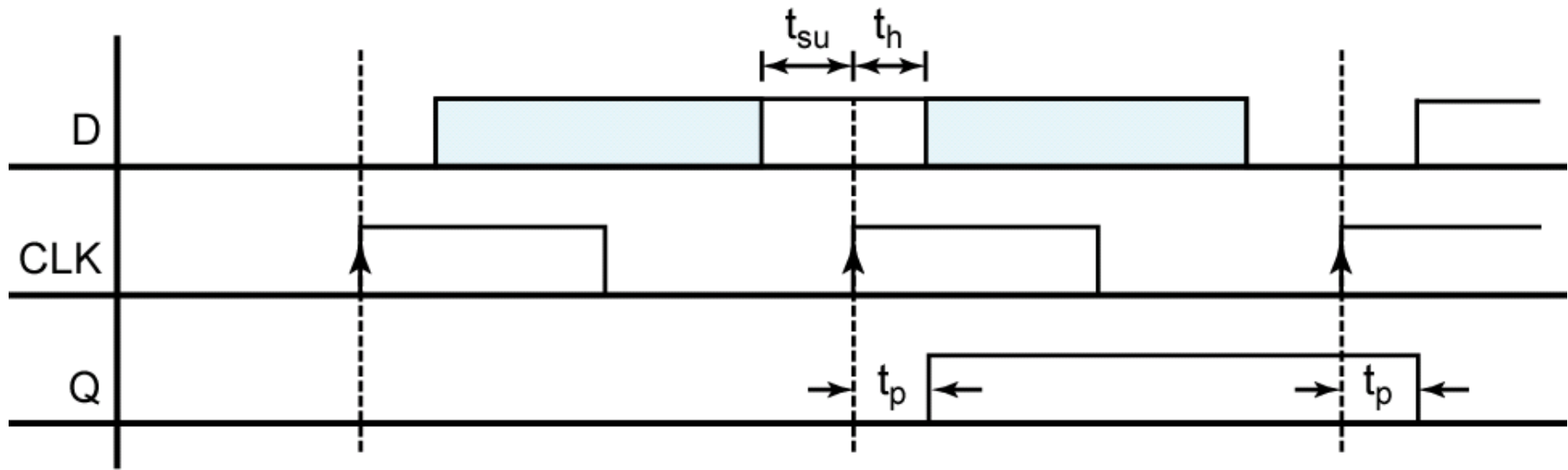


(a) Construction from two gated D latches

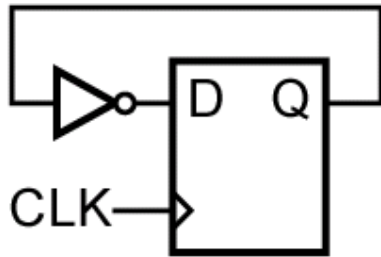


(b) Time analysis

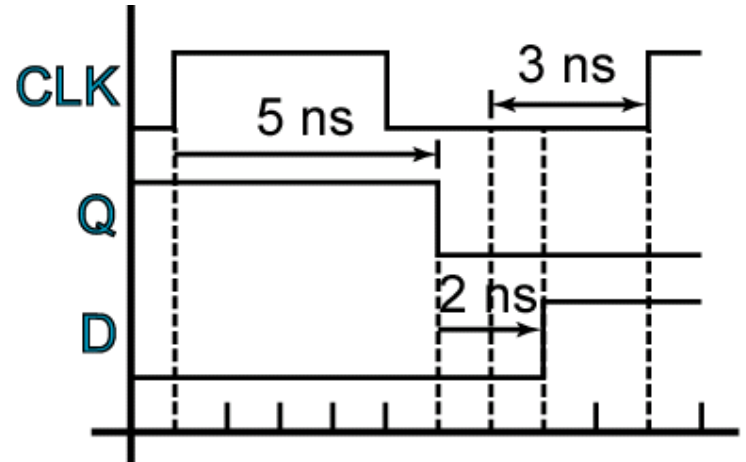
**Figure 11-15: D Flip-Flop (Rising Edge Trigger)**



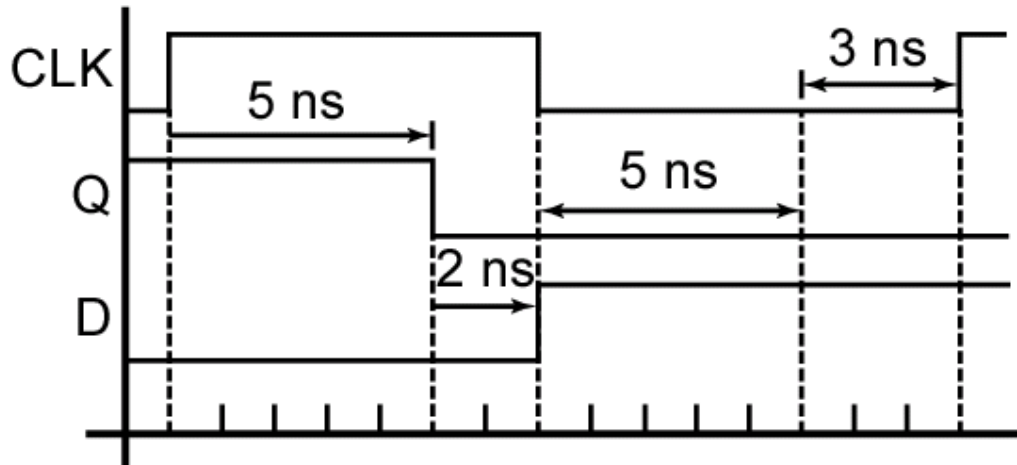
**Figure 11-16: Setup and Hold Times for an Edge-Triggered D Flip-Flop**



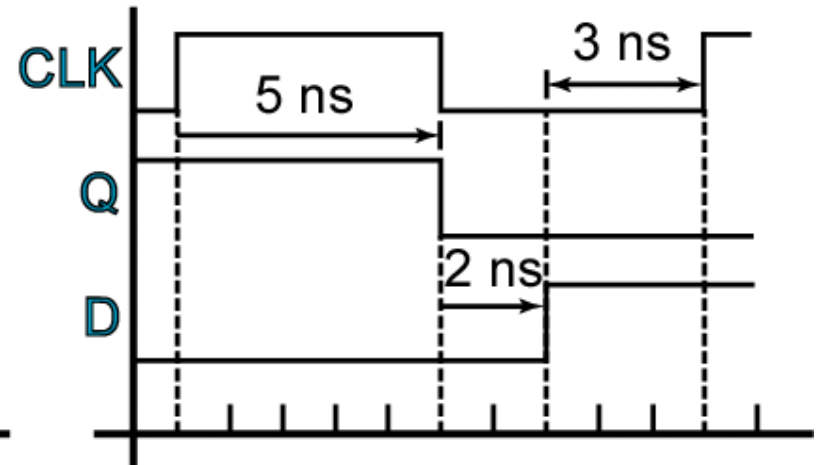
(a) Simple flip-flop circuit



(b) Setup time not satisfied



(c) Setup time satisfied



(d) Minimum clock period

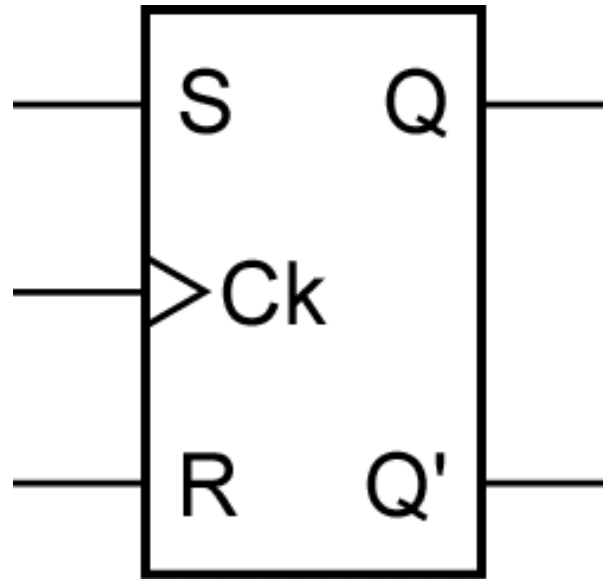
**Figure 11-17: Determination of Minimum Clock Period**

# S-R Flip-Flop

An S-R flip-flop is similar to an S-R latch in that  $S = 1$  sets the Q output to 1, and  $R = 1$  resets the Q output to 0.

The essential difference is that the flip-flop has a clock input, and the Q output can change only after an active clock edge.

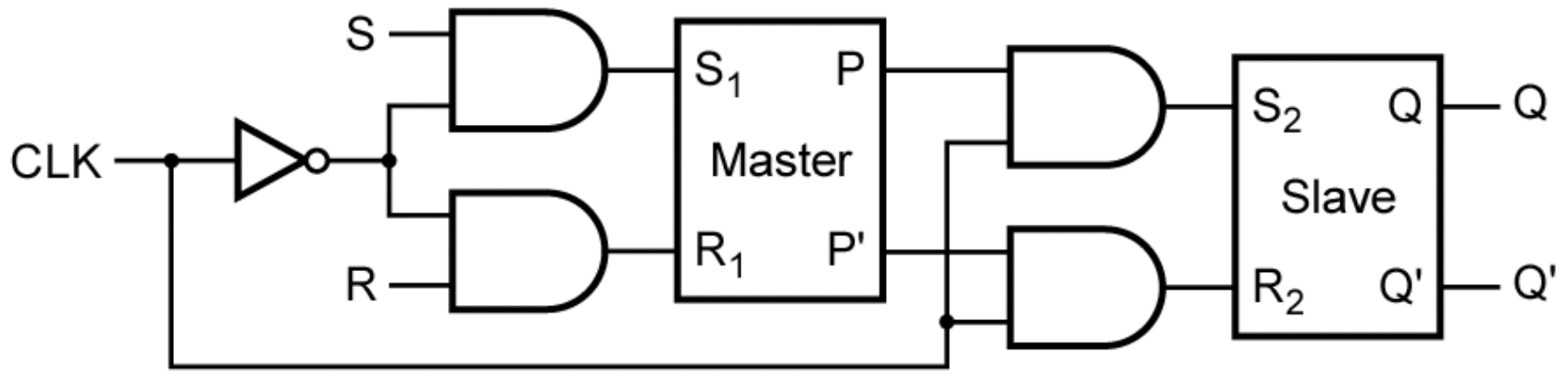
**Section 11.5 (p. 331)**



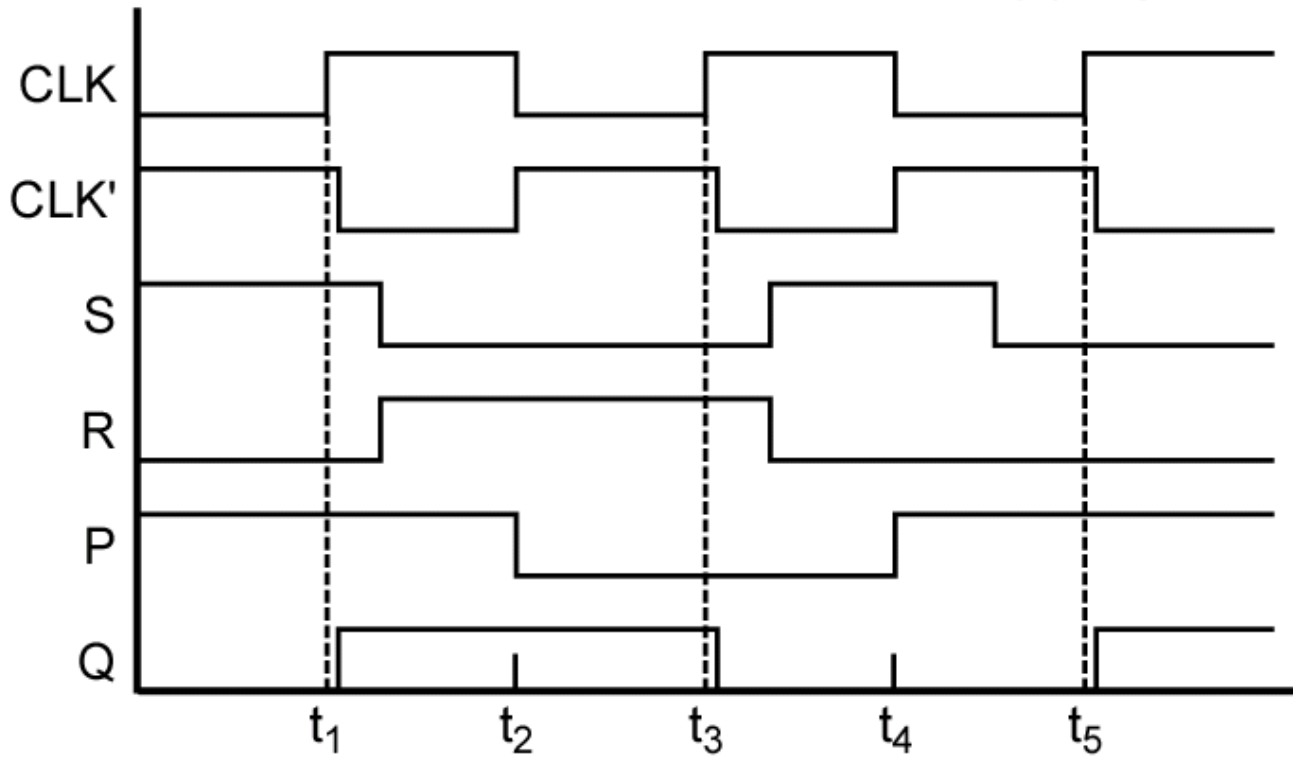
Operation summary:

- $S = R = 0$       no state change
- $S = 1, R = 0$     set  $Q$  to 1 (after active  $Ck$  edge)
- $S = 0, R = 1$     reset  $Q$  to 0 (after active  $Ck$  edge)
- $S = R = 1$       not allowed

**Figure 11-18: S-R Flip-Flop**



(a) Implementation with two latches



(b) Timing analysis

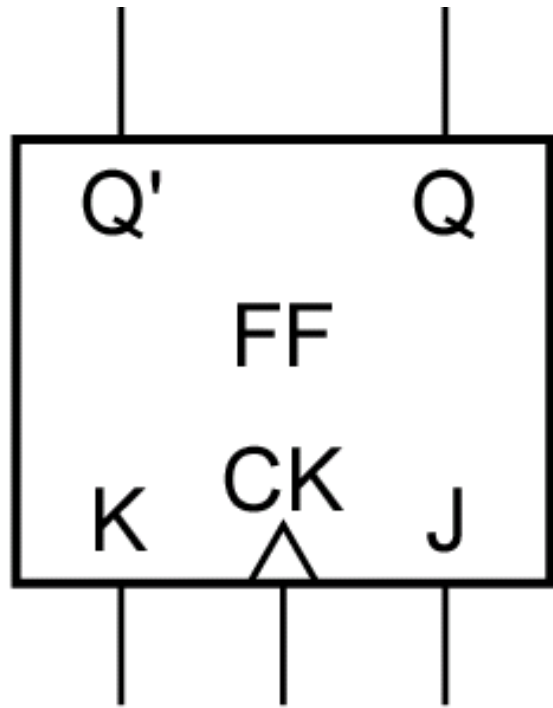
**Figure 11-19: S-R Flip-Flop Implementation and Timing**

# J-K Flip-Flop

The J-K flip-flop is an extended version of the S-R flip-flop. The J-K flip-flop has three inputs – J, K, and the clock (CK). The *J* input corresponds to *S*, and *K* corresponds to *R*.

Unlike the S-R flip-flop, a 1 input may be applied simultaneously to *J* and *K*, in which case the flip-flop changes state after the active clock edge.

**Section 11.6 (p. 332)**



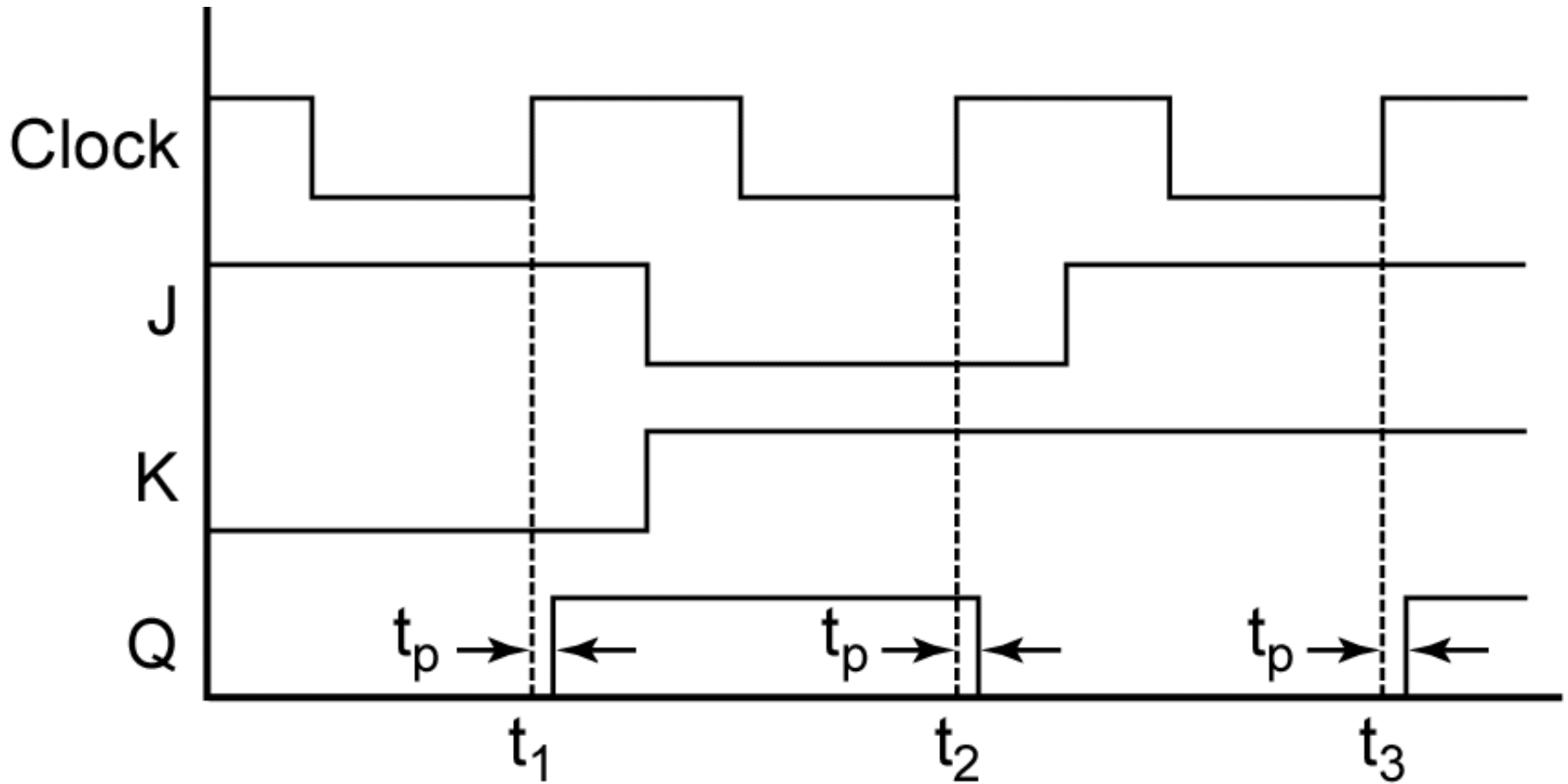
(a) J-K flip-flop

$$Q^+ = JQ' + K'Q$$

(b)

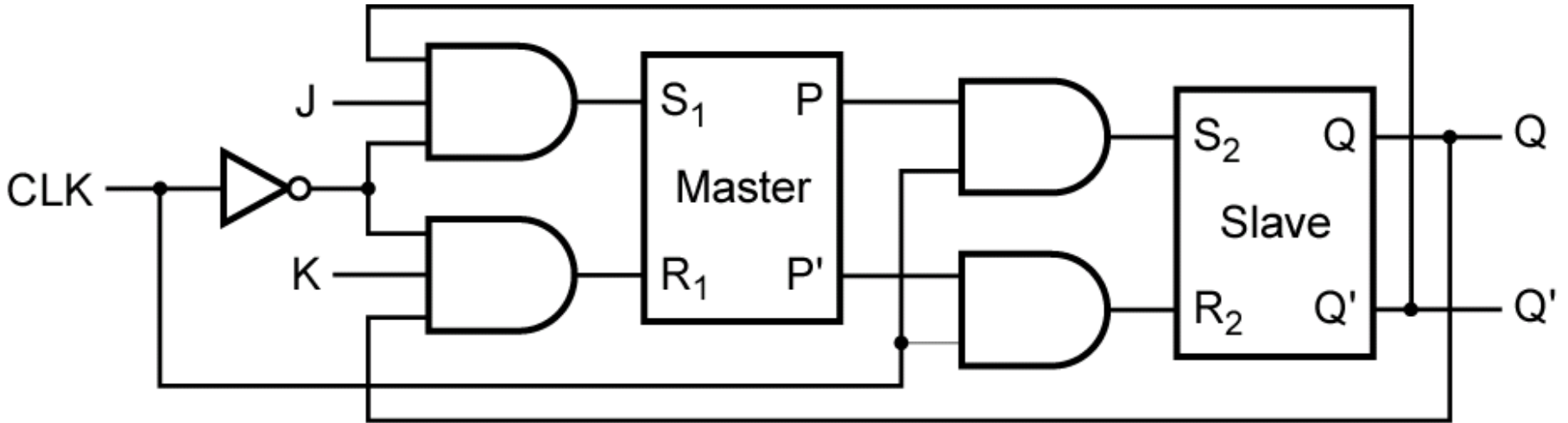
$J$	$K$	$Q$	$Q^+$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

**Figure 11-20ab: J-K Flip-Flop  
(Q Changes on the Rising Edge)**



(c) J-K flip-flop timing

**Figure 11-20c: J-K Flip-Flop  
(Q Changes on the Rising Edge)**



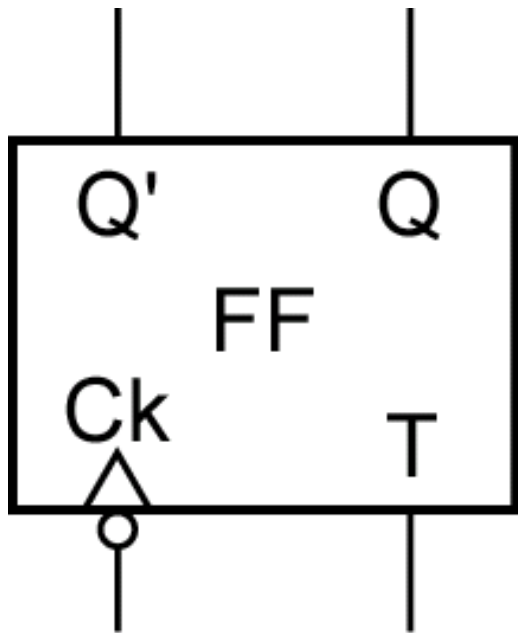
**Figure 11-21: Master-Slave J-K Flip-Flop (Q Changes on Rising Edge)**

# T Flip-Flop

The T flip-flop, also called the toggle flip-flop, is frequently used in building counters. It has a  $T$  input and a clock input.

When  $T = 1$  the flip-flop changes state after the active edge of the clock. When  $T = 0$ , no state change occurs.

**Section 11.7 (p. 333)**



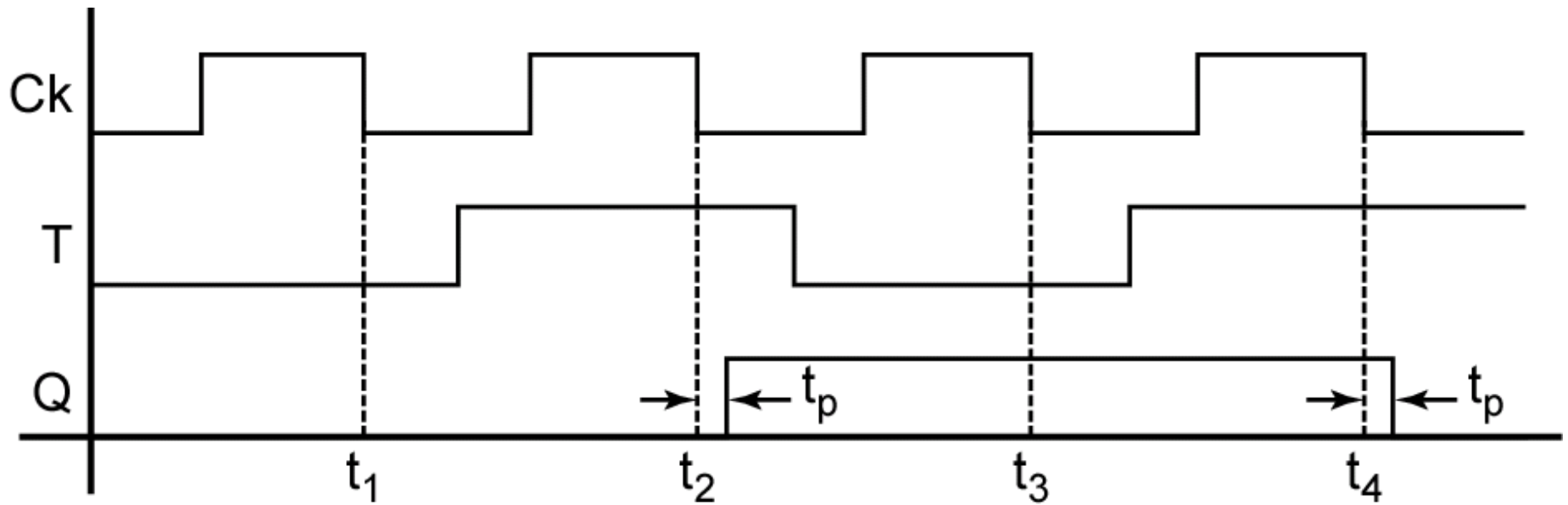
(a)

(b)

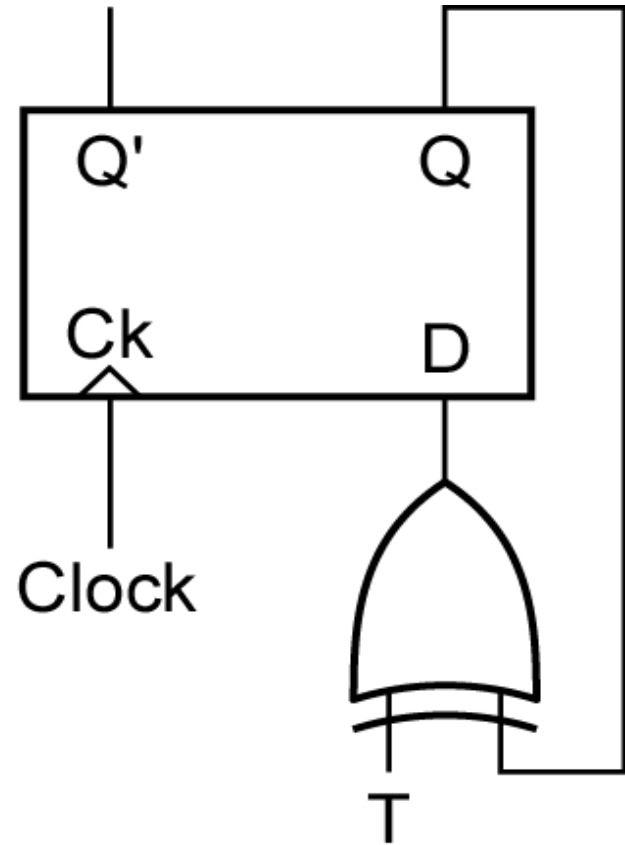
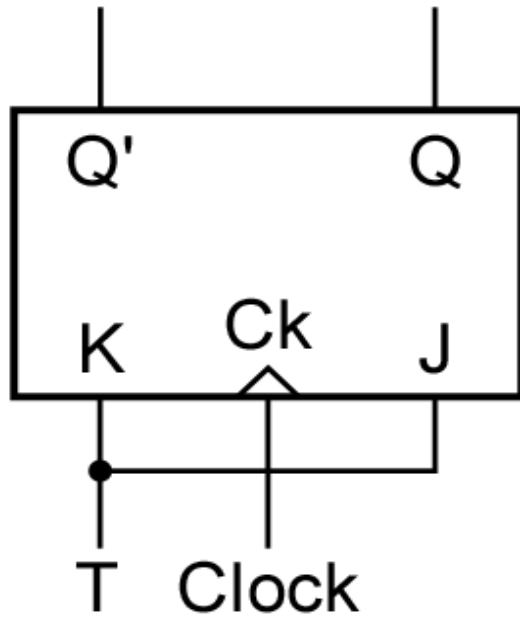
$T$	$Q$	$Q^+$
0	0	0
0	1	1
1	0	1
1	1	0

$$Q^+ = T'Q + TQ' = Q \oplus T$$

**Figure 11-22ab: T Flip-Flop**

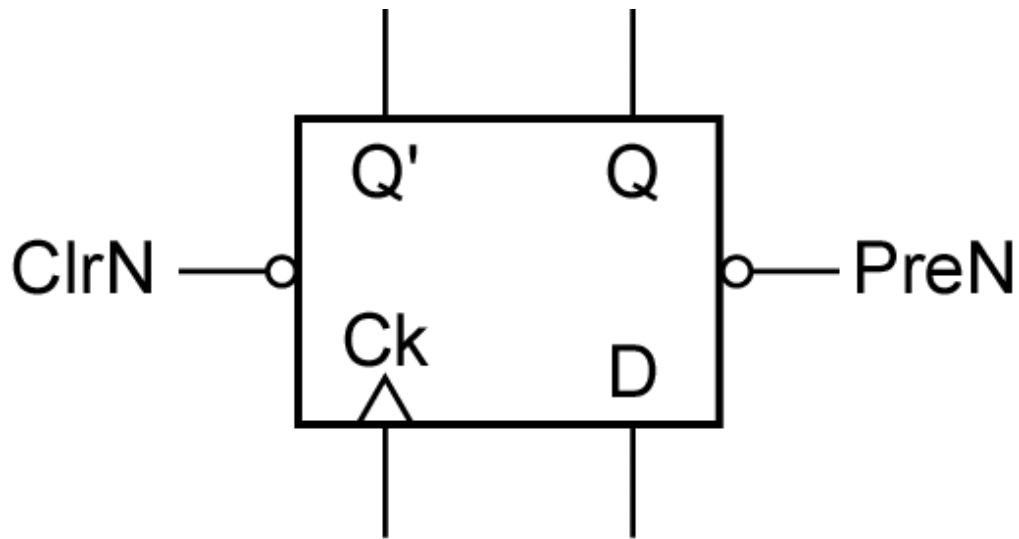


**Figure 11-23: Timing Diagram for T Flip-Flop (Falling-Edge Trigger)**



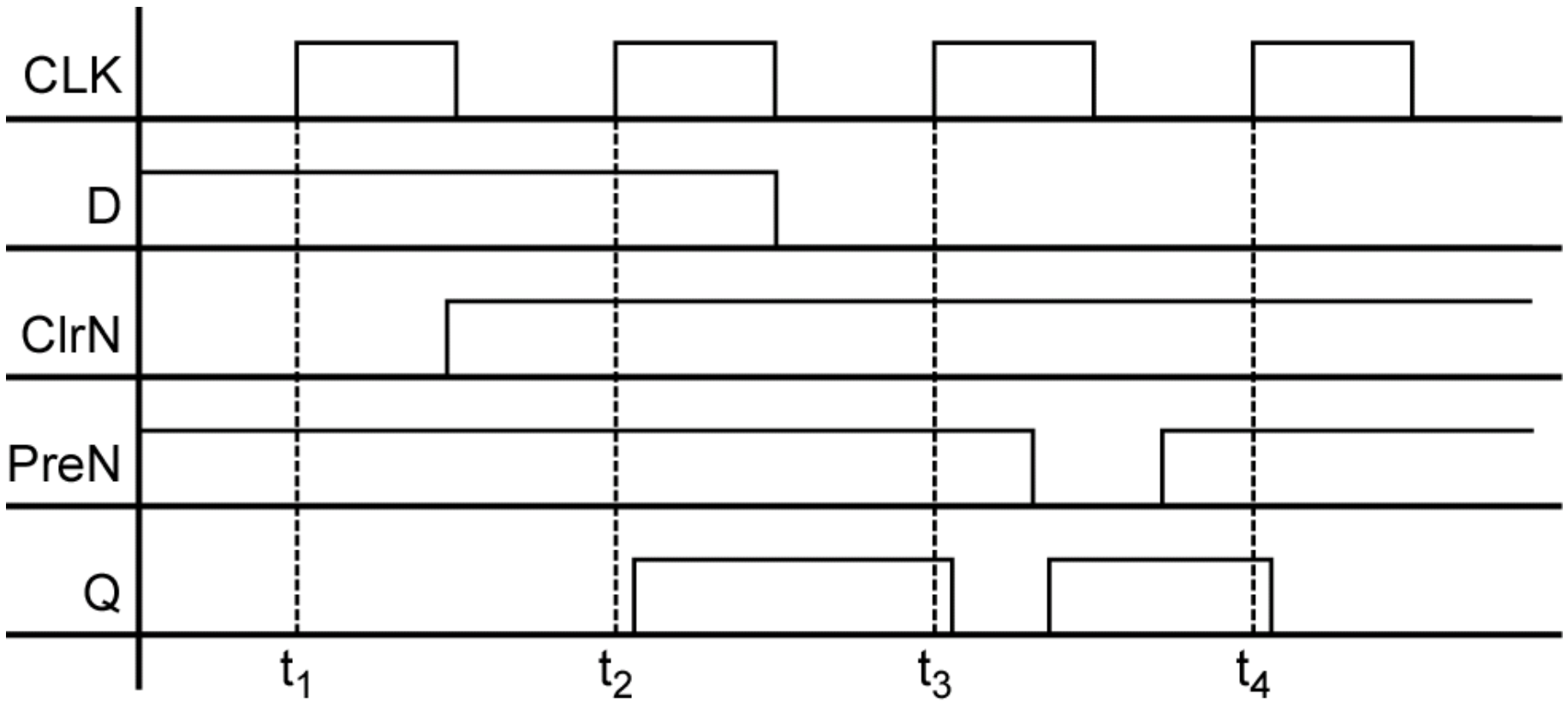
(a) Conversion of J-K to T      (b) Conversion of D to T

**Figure 11-24: Implementation of T Flip-Flops**

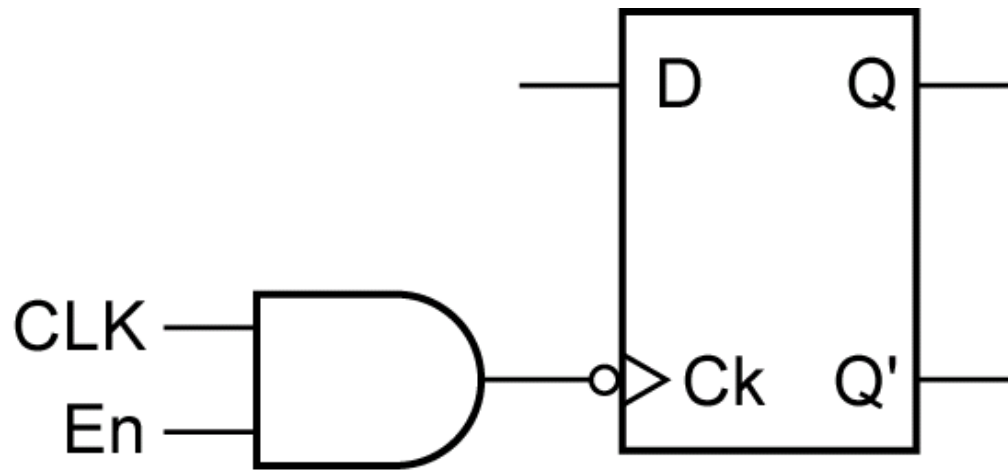


Ck	D	PreN	ClrN	$Q^+$
X	X	0	0	(not allowed)
X	X	0	1	1
X	X	1	0	0
↑	0	1	1	0
↑	1	1	1	1
0, 1, ↓	X	1	1	Q (no change)

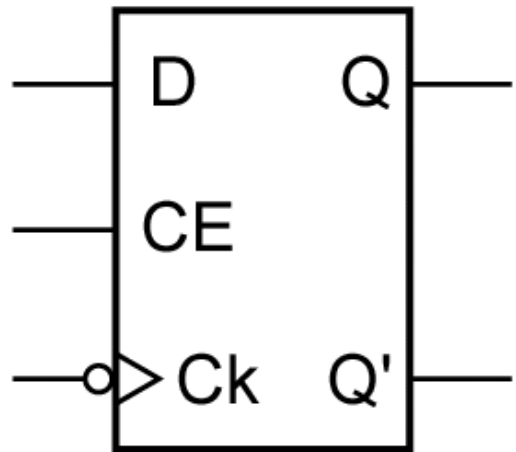
**Figure 11-25: D Flip-Flop with Clear and Preset**



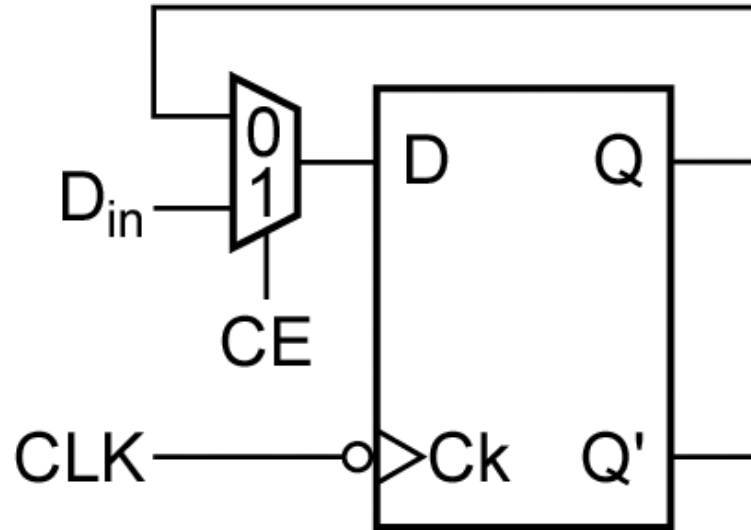
**Figure 11-26: Timing Diagram for D Flip-Flop with Asynchronous Clear and Preset**



(a) Gating the clock



(b) D-CE symbol



(c) Implementation

**Figure 11-27: D Flip-Flop with Clock Enable**